Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A data modulation method comprising the steps of:

a) converting ~~an~~ each N-bit data word of a plurality of N-bit data ~~word~~ words of a data bit stream to ~~an~~ a corresponding M-bit code word of a plurality of M-bit code words ~~and storing a plurality of said M-bit code words in a buffer~~ to form a channel bit stream, where the integer M is greater than the integer N;

b) determining a digital sum value of said channel bit stream;

c) detecting a bit sequence of a predetermined pattern in the ~~stored~~ channel bit stream; and

d) replacing a bit "1" of ~~said detected~~ the bit sequence in the channel bit stream with a bit "0" if the replacement results in said digital sum value approaching zero.

2. (Previously Presented) A data modulation method comprising the steps of:

a) mapping a plurality of 4-bit data words to a plurality of 3-bit code words in a memory;

b) segmenting a data bit stream into a plurality of 4-bit data words by successively shifting two bits at a time;

c) converting higher significant two bits of each 4-bit data word to a 3-bit code word correspondingly mapped to the 4-bit data word in said memory and converting lower significant two bits of the 4-bit data word as higher significant two bits of a subsequent 4-bit data word to a 3-bit code word correspondingly mapped to said subsequent 4-bit data word so that a channel bit stream having no consecutive 1's is produced by a plurality of said 3-bit code words;

d) determining a digital sum value of said channel bit stream;

e) detecting a first predetermined one of said 3-bit code words which is consecutive with a second predetermined one of said 3-bit code words; and

f) replacing the detected code word with a substitute code word "000" if the replacement results in said digital sum value approaching zero.

3. (Original) A data modulation method comprising the steps of:

mapping, in a memory, 2-bit data words "00", "01", "10" and "11" to 3-bit code words "101", "100", "001" and "010", respectively, and mapping 4-bit data words "0000", "0001", "1000" and "1001" to 6-bit code words "101000", "100000", "001000" and "010000", respectively;

segmenting a data bit stream into a plurality of 4-bit data words;

converting each of the 4-bit data words to a 6-bit code word mapped in said memory if the 4-bit data word is coincident with one of said mapped 4-bit data words and converting higher significant two bits of the 4-bit data word to a 3-bit code word mapped in said memory if the 4-bit data word is non-coincident with any of said mapped 4-bit data words so that a channel bit stream having no consecutive 1's is formed by a plurality of said 6-bit code words and a plurality of said 3-bit code words;

forming a subsequent 4-bit data word with lower significant bits of the non-coincident data word;

determining a digital sum value of said channel bit stream;

detecting a code word "010" which occurs immediately following any one of said 6-bit code words; and

replacing the detected code word with a substitute code word "000" if the replacement results in said digital sum value approaching zero.

4. (Original) A data modulation method comprising the steps of:

mapping, in a memory, 2-bit data words "00", "01", "10" and "11" to 3-bit code words "101", "100", "001" and "010", respectively, and mapping 4-bit data words "0000", "0001", "1000" and "1001" to 6-bit code words "101000", "100000", "001000" and "010000", respectively;

segmenting a data bit stream into a plurality of 4-bit data words;

converting each of the 4-bit data words to a 6-bit code word mapped in said memory if the 4-bit data word is coincident with one of said mapped 4-bit data words, and converting

higher significant two bits of the 4-bit data word to a 3-bit code word mapped in said memory if the 4-bit data word is non-coincident with any of said mapped 4-bit data words so that a channel bit stream having no consecutive 1's is formed by a plurality of said 6-bit code words and a plurality of said 3-bit code words;

forming a subsequent 4-bit data word with lower significant bits of the non-coincident data word;

determining a digital sum value of said channel bit stream;

detecting a code word "010000" which occurs immediately following any one of said 3-bit code words; and

replacing the detected code word with a substitute code word "000000" if the replacement results in said digital sum value approaching zero.

5. (Original) A data modulation method comprising the steps of:

mapping, in a memory, 2-bit data words "00", "01", "10" and "11" to 3-bit code words "101", "100", "001" and "010", respectively, and mapping 4-bit data words "0000", "0001", "1000" and "1001" to 6-bit code words "000101", "000100", "000001" and "000010", respectively;

segmenting a data bit stream into a plurality of 4-bit data words;

converting each of the 4-bit data words to a 6-bit code word mapped in said memory if the 4-bit data word is coincident with one of said mapped 4-bit data words, and converting higher significant two bits of the 4-bit data word to a 3-bit code word mapped in said memory if the 4-bit data word is non-coincident with any of said mapped 4-bit data words so that a channel bit stream having no consecutive 1's is formed by a plurality of said 6-bit code words and a plurality of said 3-bit code words;

forming a subsequent 4-bit data word with lower significant bits of the non-coincident data word;

determining a digital sum value of said channel bit stream;

detecting a code word "010" which is immediately followed by any one of said 6-bit code words; and

replacing the detected code word with a substitute code word "000" if the replacement results in said digital sum value approaching zero.

6. (Original) A data modulation method comprising the steps of:

mapping, in a memory, 2-bit data words "00", "01", "10" and "11" to 3-bit code words "101", "100", "001" and "010", respectively, and mapping 4-bit data words "0000", "0001", "1000" and "1001" to 6-bit code words "000101", "000100", "000001" and "000010", respectively;

segmenting a data bit stream into a plurality of 4-bit data words;

converting each of the 4-bit data words to a 6-bit code word mapped in said memory if the 4-bit data word is coincident with one of said mapped 4-bit data words;

converting higher significant two bits of the 4-bit data word to a 3-bit code word mapped in said memory if the 4-bit data word is non-coincident with any of said mapped 4-bit data words;

forming a subsequent 4-bit data word with lower significant bits of the non-coincident data word so that a channel bit stream having no consecutive 1's is formed by a plurality of said 6-bit code words and a plurality of said 3-bit code words;

determining a digital sum value of said channel bit stream;

detecting a code word "000010" which is immediately followed by any one of said 3-bit code words; and

replacing the detected code word with a substitute code word "000000" if the replacement results in said digital sum value approaching zero.

7. (Previously Presented) The data modulation method of claim 2, wherein, in said memory, a first group of 4-bit data words "001X", "01XX", "101X" and "11XX" are mapped to 3-bit code words "101", "100", "001", "010", respectively, a second group of 4-bit data words "0000", "0001", "1000" and "1001" are mapped to said 3-bit code words "101", "100", "001", "010", respectively, and a 4-bit data word "XXXX" is mapped to a 3-bit code word "000", where the symbol X represents either "1" or "0",

wherein step (c) comprises using said first and second groups of data words to convert said two higher significant bits of each 4-bit data word if said first group was used to convert two higher significant bits of an immediately preceding 4-bit data word, and using said 4-bit

data word "XXXX" to convert said two higher significant bits if said second group was used to convert said two higher significant bits of said immediately preceding 4-bit data word,

wherein step (d) comprises detecting said first predetermined 3-bit code word when the first predetermined 3-bit code word is immediately preceded by said second predetermined 3-bit code word and if said first group of data words is used to convert subsequent two higher significant bits.

8. (Original) The data modulation method of claim 7, wherein said first predetermined 3-bit code word is "010" and said second predetermined code word is "000".

9. (Previously Presented) The data modulation method of claim 1, 2, 3, 4, 5, 6, 7 or 8, further comprising the steps of detecting a bit sequence "010.101.010" in said channel bit stream and replacing the detected bit sequence with a substitute bit sequence "000. 000. 000".

10. (Previously Presented) The data modulation method of claim 1, 2, 3, 4, 5, 6, 7 or 8, wherein the step of replacing the detected code word further comprises updating said digital sum value.

11. (Previously Presented) The data modulation method of claim 1, 2, 3, 4, 5, 6, 7 or 8, further comprising the step of restoring said detected code word when a bit sequence having a predetermined number of consecutive 0's is formed in said channel bit stream due to the replacement of said detected code with said substitute code word "000".

12. (Previously Presented) The data modulation method of claim 1, 2, 3, 4, 5, 6, 7 or 8, further comprising the steps of generating a synchronization pattern and inserting the synchronization pattern to said channel bit stream.

13. (Original) The data modulation method of claim 12, wherein said synchronization pattern comprises a bit sequence "000. 000. 000."

14. (Previously Presented) The data modulation method of claim 1, 2, 3, 4, 5, 6, 7 or 8, further comprising the steps of:

storing a plurality of synchronization patterns in a memory;

selecting one of the synchronization patterns according to the amount of offset from starting point of a sector on a recording disc; and

inserting the selected synchronization pattern to said channel bit stream.

15. (Original) The data modulation method of claim 14, wherein each of said synchronization patterns comprises a bit sequence "000. 000. 000."

16. (Previously Presented) The data modulation method of claim 1, 2, 3, 4, 5, 6, 7 or 8, further comprising the steps of:

storing, in a memory, a first group of synchronization patterns of even-number of 1's and a second group of synchronization patterns of odd-number of 1's;

selecting one of the synchronization patterns of even-number of 1's from said first group and one of the synchronization patterns of odd-number of 1's from said second group according to the amount of offset from starting point of a sector on a recording disc;

choosing one of the selected synchronization patterns of even-number of 1's and odd-number of 1's so that the chosen synchronization pattern results in said digital sum value approaching zero; and

inserting the chosen synchronization pattern to said channel bit stream.

17. (Original) The data modulation apparatus of claim 16, wherein each of said synchronization patterns comprises a bit sequence "000. 000. 000."

18. (Previously Presented) The data modulation method of claim 1, 2, 3, 4, 5, 6, 7 or 8, further comprising the steps of:

mapping a plurality of code words to a plurality of data words in a memory;

receiving said channel bit stream and detecting a bit sequence "000. 000" in the received channel bit stream;

replacing the detected bit sequence with a substitute bit sequence; and

converting each code word of the channel bit stream to a data word corresponding to one of the data words mapped in said memory.

19. (Original) The data modulation method of claim 18, wherein said substitute bit sequence is "010. 000".

20. (Original) The data modulation method of claim 18, wherein said substitute bit sequence is "000. 010".

21. (Original) The data modulation method of claim 18, wherein the replacing step further comprises detecting a bit sequence "000. 000. 000" and replacing the detected bit sequence with a bit sequence "010. 101. 010".

22. (Original) The data modulation method of claim 18, wherein a plurality of 3-bit code words are mapped in said memory to a plurality of 2-bit data words and a plurality of 6-bit code words are mapped to a plurality of 4-bit data words.

23. (Currently Amended) A data modulation apparatus comprising:

~~a buffer;~~

conversion circuitry for converting ~~an~~ each N-bit data word of a plurality of N-bit data ~~word~~ words of a data bit stream to ~~an~~ a corresponding M-bit code word of a plurality of M-bit code words ~~and storing a plurality of said M-bit code words in said buffer~~ to form a channel bit stream, where the integer M is greater than the integer N; and

control circuitry for determining a digital sum value of said channel bit stream, and for detecting a bit sequence of a predetermined pattern in the ~~stored~~ channel bit stream, and for replacing a bit "1" of ~~said detected~~ the bit sequence in the channel bit stream with a bit "0" if the replacement results in said digital sum value approaching zero.

24. (Previously Presented) A data modulation apparatus comprising:

a memory for mapping a plurality of 4-bit data words to a plurality of 3-bit code words;

conversion circuitry for segmenting a data bit stream into a plurality of 4-bit data words and successively shifting two bits at a time, converting higher significant two bits of each 4-bit data word to a 3-bit code word correspondingly mapped to the 4-bit data word in said memory and converting lower significant two bits of the 4-bit data word as higher significant two bits of a subsequent 4-bit data word to a 3-bit code word correspondingly mapped to said subsequent 4-bit data word so that a channel bit stream having no consecutive 1's is produced by a plurality of said 3-bit code words; so that a channel bit stream having no consecutive 1's is produced by a plurality of said 3-bit code words; and

control circuitry for determining a digital sum value of said channel bit stream, detecting a first predetermined one of said 3-bit code words which is consecutive with a second predetermined one of said 3-bit code words, and replacing the detected code word with a substitute ode word "000" if the replacement results in said digital sum value approaching zero.

25. (Original) A data modulation apparatus comprising:

a memory for mapping 2-bit data words "00", "01", "10" and "11" to 3-bit code words "101", "100", "001" and "010", respectively, and mapping 4-bit data words "0000", "0001", "1000" and "1001" to 6-bit code words "101000", "100000", "001000" and "010000", respectively;

conversion circuitry for successively segmenting a data bit stream into a plurality of 4-bit data words, converting each of the 4-bit data words to a 6-bit code word mapped in said memory if the 4-bit data word is coincident with one of said mapped 4-bit data words, converting higher significant two bits of the 4-bit data word to a 3-bit code word mapped in said memory if the 4-bit data word is non-coincident with any of said mapped 4-bit data words, and forming a subsequent 4-bit data word with lower significant bits of the non-coincident data word so that a channel bit stream having no consecutive 1's is formed by a plurality of said 6-bit code words and a plurality of said 3-bit code words; and

control circuitry for determining a digital sum value of said channel bit stream, detecting a code word "010" which occurs immediately following any one of said 6-bit code words, and replacing the detected code word with a substitute code word "000" if the replacement results in said digital sum value approaching zero.

26. (Original) A data modulation apparatus comprising:

a memory for mapping 2-bit data words "00", "01", "10" and "11" to 3-bit code words "101", "100", "001" and "010", respectively, and mapping 4-bit data words "0000", "0001", "1000" and "1001" to 6-bit code words "101000", "100000", "001000" and "010000", respectively;

conversion circuitry for successively segmenting a data bit stream into a plurality of 4-bit data words, converting each of the 4-bit data words to a 6-bit code word mapped in said memory if the 4-bit data word is coincident with one of said mapped 4-bit data words, converting higher significant two bits of the 4-bit data word to a 3-bit code word mapped in said memory if the 4-bit data word is non-coincident with any of said mapped 4-bit data words, and forming a subsequent 4-bit data word with lower significant bits of the non-coincident data word so that a channel bit stream having no consecutive 1's is formed by a plurality of said 6-bit code words and a plurality of said 3-bit code words; and

control circuitry for determining a digital sum value of said channel bit stream, detecting a code word "010000" which occurs immediately following any one of said 3-bit code words, and replacing the detected code word with a substitute code word "000000" if the replacement results in said digital sum value approaching zero.

27. (Original) A data modulation apparatus comprising:

a memory for mapping 2-bit data words "00", "01", "10" and "11" to 3-bit code words "101", "100", "001" and "010", respectively, and mapping 4-bit data words "0000", "0001", "1000" and "1001" to 6-bit code words "000101", "000100", "000001" and "000010", respectively;

conversion circuitry for successively segmenting a data bit stream into a plurality of 4-bit data words, converting each of the 4-bit data words to a 6-bit code word mapped in said memory if the 4-bit data word is coincident with one of said mapped 4-bit data words, converting higher significant two bits of the 4-bit data word to a 3-bit code word mapped in said memory if the 4-bit data word is non-coincident with any of said mapped 4-bit data words, and forming a subsequent 4-bit data word with lower significant bits of the non-

coincident data word so that a channel bit stream having no consecutive 1's is formed by a plurality of said 6-bit code words and a plurality of said 3-bit code words; and

control circuitry for determining a digital sum value of said channel bit stream, detecting a code word "010" which is immediately followed by any one of said 6-bit code words, and replacing the detected code word with a substitute code word "000" if the replacement results in said digital sum value approaching zero.

28. (Original) A data modulation apparatus comprising:

a memory for mapping 2-bit data words "00", "01", "10" and "11" to 3-bit code words "101", "100", "001" and "010", respectively, and mapping 4-bit data words "0000", "0001", "1000" and "1001" to 6-bit code words "000101", "000100", "000001" and "000010", respectively;

conversion circuitry for successively segmenting a data bit stream into a plurality of 4-bit data words, converting each of the 4-bit data words to a 6-bit code word mapped in said memory if the 4-bit data word is coincident with one of said mapped 4-bit data words, converting higher significant two bits of the 4-bit data word to a 3-bit code word mapped in said memory if the 4-bit data word is non-coincident with any of said mapped 4-bit data words, and forming a subsequent 4-bit data word with lower significant bits of the non-coincident data word so that a channel bit stream having no consecutive 1's is formed by a plurality of said 6-bit code words and a plurality of said 3-bit code words; and

control circuitry for determining a digital sum value of said channel bit stream, detecting a code word "000010" which is immediately followed by any one of said 3-bit code words, and replacing the detected code word with a substitute code word "000000" if the replacement results in said digital sum value approaching zero.

29. (Previously Presented) The data modulation apparatus of claim 24, wherein said memory maps a first group of 4-bit data words "001X", "01XX", "101X" and "11XX" to 3-bit code words "101", "100", "001", "010", respectively, maps a second group of 4-bit data words "0000", "0001", "1000" and "1001" to said 3-bit code words "101", "100", "001", "010", respectively, and maps a 4-bit data word "XXXX" to a 3-bit code word "000", where the symbol X represents either "1" or "0",

wherein said conversion circuitry uses said first and second groups of data words to convert said two higher significant bits of each 4-bit data word if said first group was used to convert two higher significant bits of an immediately preceding 4-bit data word, and uses said 4-bit data word "XXXX" for converting said two higher significant bits if said second group was used to convert two higher significant bits of said immediately preceding 4-bit data word,

wherein said control circuitry detects said first predetermined 3-bit code word when the first predetermined 3-bit code word is immediately preceded by said second predetermined 3-bit code word and if said first group of data words is used to convert subsequent two higher significant bits.

30. (Original) The data modulation apparatus of claim 29, wherein said first predetermined 3-bit code word is "010" and said second predetermined code word is "000".

31. (Previously Presented) The data modulation apparatus of claim 23, 24, 25, 26, 27, 28, 29 or 30, further comprising a replacement circuit for detecting a bit sequence "010. 101. 010" in said channel bit stream and replacing the detected bit sequence with a substitute bit sequence "000. 000. 000".

32. (Previously Presented) The data modulation apparatus of claim 23, 24, 25, 26, 27, 28, 29 or 30, wherein said control circuitry updates said digital sum value after the detected code word is replaced with said code word "000".

33. (Previously Presented) The data modulation apparatus of claim 23, 24, 25, 26, 27, 28, 29 or 30, wherein said control circuitry restores said detected code word when a bit sequence having a predetermined number of consecutive 0's is formed in said channel bit stream due to the replacement of said detected code with said substitute code word "000".

34. (Previously Presented) The data modulation apparatus of claim 23, 24, 25, 26, 27, 28, 29 or 30, further comprising means for generating a synchronization pattern and inserting the synchronization pattern to said channel bit stream.

35. (Original) The data modulation apparatus of claim 34, wherein said synchronization pattern comprises a bit sequence "000. 000. 000."

36. (Previously Presented) The data modulation apparatus of claim 23, 24, 25, 26, 27, 28, 29 or 30, further comprising:

a memory for storing a plurality of synchronization patterns;

means for selecting one of the synchronization patterns according to the amount of offset from starting point of a sector on a recording disc; and

means for inserting the selected synchronization pattern to said channel bit stream.

37. (Original) The data modulation apparatus of claim 36, wherein each of said synchronization patterns comprises a bit sequence "000. 000. 000."

38. (Previously Presented) The data modulation apparatus of claim 23, 24, 25, 26, 27, 28, 29 or 30, further comprising:

a memory for storing a first group of synchronization patterns of even-number of 1's and a second group of synchronization patterns of odd-number of 1's;

means for selecting one of the synchronization patterns of even-number of 1's from said first group and one of the synchronization patterns of odd-number of 1's from said second group according to the amount of offset from starting point of a sector on a recording disc;

means for choosing one of the selected synchronization patterns of even-number of 1's and odd-number of 1's so that the chosen synchronization pattern results in said digital sum value approaching zero; and

means for inserting the chosen synchronization pattern to said channel bit stream.

39. (Original) The data modulation apparatus of claim 38, wherein each of said synchronization patterns comprises a bit sequence "000. 000. 000."

40. (Previously Presented) The data modulation apparatus of claim 23, 24, 25, 26, 27, 28, 29 or 30, further comprising:

replacement circuitry for receiving said channel bit stream and detecting a bit sequence "000. 000" in the received channel bit stream, and replacing the detected bit sequence with a substitute bit sequence;

a memory for mapping a plurality of code words to a plurality of data words; and

conversion circuitry for receiving the channel bit stream from said replacement circuitry and converting each code word of the channel bit stream to a data word corresponding to one of the mapped data words of said memory.

41. (Original) The data modulation apparatus of claim 40, wherein said substitute bit sequence is "010. 000".

42. (Original) The data modulation apparatus of claim 40, wherein said substitute bit sequence is "000. 010".

43. (Original) The data modulation apparatus of claim 40, wherein said replacement circuit further detects a bit sequence "000. 000. 000" and replacing the detected bit sequence with a bit sequence "010. 101. 010".

44. (Original) The data modulation apparatus of claim 40, wherein said memory maps a plurality of 3-bit code words to a plurality of 2-bit data words and maps a plurality of 6-bit code words to a plurality of 4-bit data words.